

patenting. Applicant assumes that a double patenting rejection is being applied. The provisional rejection based on double patenting is respectfully traversed.

35 U.S.C. §101 prevents two patents from issuing on the same invention. The use of "same invention" means that identical subject matter must be claimed. The subject matter of claims 1-25 for U.S. Patent Application No. 09/911,409 is not identical to the subject matter for claims 1-32 of this application.

Independent claims 1, 27 and 28 recite a first port, a second port and a reception circuit. The independent claims also recite a RAM, a first control circuit and a second control circuit that are associated with the first port, the second port and the reception circuit. None of the claims for U.S. Patent Application No. 09/911,409 recite a first port, a second port or a reception circuit. Claims 1, 20 and 21 (cited in the Office Action) of U.S. Patent No. 09/911,409 recite first and second bus lines. The first and second bus lines are not the same as first and second ports as recited in claims 1, 27 and 28 for this application. The claims for U.S. Patent Application No. 09/911,409 also fail to recite any structure that corresponds to a reception circuit.

Claims 1-25 for U.S. Patent Application No. 09/911,409 thus fail to recite the same invention as claims 1-32 for this application. It is respectfully requested that the provisional rejection be withdrawn.

Claims 1, 6, 21 and 26-32 were rejected under 35 U.S.C. §103(a) over Kida et al. (Kida), U.S. Patent No. 6,335,728 in view of Shimamoto, U.S. Patent No. 6,147,672. The rejection is respectfully traversed.

Kida and Shimamoto fail to disclose or suggest a RAM-incorporated driver with a first port through which still-image data or a given command is input from an external MPU and a second port through which the moving-image data, which is transferred serially over a

serial transfer line from the external MPU, is input as a differential signal, as recited in claim 1.

Kida fails to disclose all of the features recited in claim 1 because Kida fails to disclose an MPU that is external to a RAM-incorporated driver. Kida discloses a plasma display apparatus (Fig. 7) that has a driving apparatus. The driving apparatus includes an A/D converter 31, a control circuit 32 and an image processing circuit 33 (col. 10, lines 12-25). Each of the field memories 34A, 34B has a capacity that is capable of storing at least the pixel data of one field. The field memories 34A, 34B are connected to the image data processing circuit 33 via switches SW31, SW32 which are serially connected (col. 10, lines 26-30).

Page 4 of the Office Action associates the data processing unit 33 and the control circuit 32 as components that are external to the remaining structure of Fig. 7. However, as clearly shown in Fig. 7 of Kida, the control circuit 32 and the data processing circuit 33 are not external components. The switches SW31, SW32 thus do not receive an input from an external MPU because the data processing circuit 33 and the control circuit 32 form a part of the driving apparatus.

Shimamoto fails to overcome the deficiencies of Kida because Shimamoto also fails to disclose an external MPU. Shimamoto is only relied upon to suggest a reception circuit. Shimamoto fails to disclose inputting still-image data or moving-image data from an external MPU.

Kida and Shimamoto also fail to disclose a RAM-incorporated driver with a second port that is independent from a first port, as recited in claims 27 and 28. As shown in Fig. 7 of Kida, the switches SW31, SW32 are serially connected and thus clearly not independent.

Kida and Shimamoto also fail to disclose or suggest a RAM which stores the still-image data that was input through the first port and the moving-image data that was created

by the reception circuit and a first control circuit and a second control circuit that operate using the RAM, as recited in claim 1 and as similarly recited in claims 27 and 28.

In Kida, two field memories 34A, 34B are connected to a data processing circuit 33 via the switches SW31, SW32. As such, a single field memory is not used to store still-image data and moving-image data. Kida's structure is thus complicated compared to the structure of claims 1, 27 and 28 because the control circuits of Kida operate using data stored in two separate memories rather than a single RAM as recited in claims 1, 27 and 28.

Kida and Shimamoto thus fail to disclose or suggest all of the features recited in claims 1, 27 and 28 as well as the additional features recited in the dependent claims thereof. It is respectfully requested that the rejection be withdrawn.

Claims 2-5, 7-10 and 22-25 were rejected under 35 U.S.C. §103(a) over Kida in view of Shimamoto and Chida, U.S. Patent No. 6,313,863 and claims 11-20 were rejected under 35 U.S.C. §103(a) over Kida in view of Shimamoto and Silverman et al, (Silverman), U.S. Patent No. 6,370,603. The rejections are respectfully traversed.

Chida and Silverman fail to overcome the deficiencies of Kida and Shimamoto because Chida and Silverman also fail to disclose the external MPU of claim 1, the first and second ports of claims 27 and 28 and the RAM of claims 1, 27 and 28.

Accordingly, none of the applied references disclose or suggest all of the features recited in claims 1, 27 and 28 as well as the additional features recited in claims 2-5, 7-20 and 22-25. It is respectfully requested that the rejections be withdrawn.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-32 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Scott M. Schulte
Registration No. 44,325

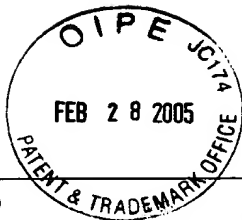
JAO:SMS/sxb

Attachment:
Substitute Form PTO-1449

Date: February 28, 2005

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

<p>DEPOSIT ACCOUNT USE AUTHORIZATION Please grant any extension necessary for entry; Charge any fee due to our Deposit Account No. 15-0461</p>

Sheet 1 of 1Form PTO-1449
(REV. 8-83)US Dept. of Commerce
PATENT & TRADEMARK OFFICEATTY DOCKET NO.
110196APPLICATION NO.
09/911,829

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

APPLICANT(S)
Tsuyoshi TAMURAFILING DATE
July 25, 2001GROUP
2674

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	-1	6,329,973 B1	12/11/01	AKIMOTO ET AL.		

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	2	JP-A-9-281933 (w/Abstr & Trans)	10/31/1997	JAPAN		
	3	JP-A-7-92953 (w/Abstr & Trans)	4/7/1995	JAPAN		
	4	JP-A-6-130910 (w/Abstr & Trans)	5/13/1994	JAPAN		
	5	JP-A-9-34426 (w/Abstr & Trans)	2/7/1997	JAPAN		
	6	WO 97/11447	3/27/1997	WIPO		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER

DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: January 13, 2005